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PARALLEL APPLICATION POWER AND PERFORMANCE PREDICTION MODELING USING SIMULATION

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ABSTRACT

High performance computing (HPC) system runs compute-intensive parallel applications requiring large number of nodes. An HPC system consists of heterogeneous computer architecture nodes, including CPUs, GPUs, field programmable gate arrays (FPGAs), etc. Power capping is a method to improve parallel application performance subject to variable power constraints. In this paper, we propose a parallel application power and performance prediction simulator. We present prediction model to predict application power and performance for unknown power-capping values considering heterogeneous computing architecture. We develop a job scheduling simulator based on parallel discrete-event simulation engine. The simulator includes a power and performance prediction model, as well as a resource allocation model. Based on real-life measurements and trace data, we show the applicability of our proposed prediction model and simulator.

1 INTRODUCTION

Scientific applications with high computation requirements are generally executed on large-scale computing platforms, such as high-performance computing (HPC) systems. HPC systems consume significant power during their operations, often in the range of tens of megawatts of power. For example, the current top-ranked Fugaku supercomputer consumes approximately 29MWs of power to reach 442 PetaFlops compute capability (Dongarra, Jack 2020). In particular, the HPC community in the United States is faced with the challenge of maintaining the energy consumption of the exascale systems within 20MWs. However, majority of the supercomputers in the top positions in terms of computing capability consume power in the megawatts range (Dongarra and Luszczek 2011). Therefore, energy consumption reduction has been identified as a major challenge for current and future HPC systems.

Different energy saving techniques, including job scheduling algorithms and resource provisioning methods, have been proposed to reduce HPC system energy consumption. Power capping has shown to be an effective technique to achieve overall power and performance optimization of parallel application

running on HPC platform (Lefurgy et al. 2008; Cochran et al. 2011; Sarood et al. 2013; Wu et al. 2016). Power capping method limits the power allocation to the nodes to achieve predefined power threshold for the node. Power capping capability is becoming a standard feature for modern processors through various programming interfaces, such as Intel's running average power limit (RAPL), AMD's advanced power management link (APML), and NVIDIA's NVIDIA management library (NVML).

HPC system contains heterogeneous computing architecture, such as CPUs, GPUs and field-programmable gate arrays (FPGAs). Accelerator architectures such as GPUs and FPGAs are designed in a different design principle, and hence consume power differently than CPUs. Moreover, power and performance characteristic profile of GPU and FPGA nodes tend to be different than CPU nodes. In this paper, we consider power capping effect on heterogeneous computer architecture, and develop prediction and simulation model for parallel applications running on HPC platform. More specifically, our contributions in the paper can be summarized as follows:

- We propose a simulator for HPC application power and performance prediction and simulation. The simulator is developed based on a parallel discrete event simulation engine. The simulator includes an application power and performance prediction model, as well as a resource allocation model. The prediction model can be used to predict application power and performance for various power-capping values. The resource allocation model can optimize power capping allocation for HPC applications.
- We demonstrate the effectiveness of our proposed simulator on various heterogeneous computing platform (e.g., CPUs, GPUs, FPGAs). We present four case studies. First case study focuses on CPU power consumption based on real-life measurements. The next two studies focus on GPU and FPGA power consumption based on collected trace data. The final case study demonstrates the resource optimization of heterogeneous computing platform.

The rest of this paper is organized as follows. In Section 2, we discuss the related studies that are most pertinent to this work. In Section 3, we present a job scheduling simulator based on discrete event simulation engine. In the same section, we present prediction model for power and performance for various power-capping values. In Section 4, we present results from different case studies to show effectiveness of the simulator. In Section 5, we conclude our paper.

2 RELATED WORK

In this section, we present related work. We first discuss power and performance prediction models for HPC applications. We then present various resource allocation methods in HPC systems. Finally, we discuss HPC job scheduling simulators.

2.1 Power and Performance Prediction

Many power and performance prediction models for parallel applications have been proposed in the literature. For example, Singh et al. (Singh et al. 2009) proposed an analytical model for real-time prediction of processor and system power consumption. Performance monitoring counters are used to estimate the power consumption of the processors. FlexCL (Liang et al. 2018) is an analytical power and performance prediction model for OpenCL workloads on FPGAs. FlexCL performs static analysis to transform the OpenCL kernel to control data flow graph (CDFG), and then estimates performance for basic blocks. Olschanowsky et al. (Olschanowsky et al. 2010) proposed energy prediction for non-existent machines using existing application traces with performance counters. The method requires instrumentation of the applications (at the basic block level) and predicts the total energy cost based on the average energy cost at each operation. Song et al. (Song et al. 2013) proposed a unified quasi-analytical performance and power model. Their model combines application analysis with different computation and communication parameters obtained through micro-benchmarking to assess the impact of different applications on performance and energy

efficiency of HPC systems. Recently, Heinrich et al. (Heinrich et al. 2017) proposed model to predict the energy consumption of MPI applications via simulation. The model can be calibrated from a single node of a cluster to predict energy consumption on the entire cluster. Saillant et al. (Saillant et al. 2020) presented power prediction model based on the job submission data. In this paper, we propose a job simulator to predict application characteristics (e.g., power, performance) based on various power-capping values on heterogeneous computing architecture.

2.2 Resource Allocation

Different energy saving techniques have been proposed for HPC systems, such as power capping, dynamic voltage and frequency scaling (DVFS), auto-tuning, among others. Energy-saving methods that exploit the dynamic voltage and frequency scaling (DVFS) capabilities on processors have been introduced (e.g., (Ge et al. 2007; Rountree et al. 2009; Bao et al. 2016)). CPU MISER (Ge et al. 2007) is an early effort that includes a runtime DVFS-based HPC power management scheme, which exploits different application phases using performance measurements (in cycles per instruction) during the execution of the applications. Adagio (Rountree et al. 2009) performs runtime CPU frequency scaling and exploits the variations in the energy consumption during computation and communication phases of an application to reduce the overall energy consumption without impacting the overall execution time of the application. A more recent effort on DVFS by Bao et al. (Bao et al. 2016) automatically selects the optimal frequency and core count at compile-time to achieve lower energy. Furthermore, Sourouri et al. (Sourouri et al. 2017) combined autotuning of applications with DVFS technique to achieve energy-efficiency in HPC and embedded systems.

Power capping is the allocation of power to nodes mainly to achieve an overall HPC cluster power limit. Power capping not only helps achieve power reduction in the node but also optimizes application performance within a power budget. Hardware-level power capping is a lucrative choice, since it gives the highest opportunity to save energy. As such, many recent studies have focused on achieving optimized energy consumption through exploiting power capping capability (Sarood et al. 2013; Liu et al. 2016; Ahmed et al. 2018). Recently, much interest has been shown for job scheduling and resource allocation to HPC jobs in power bound HPC systems. Sarood et al. explored the possibility of exploiting power capping capability of processor and memory subsystems in HPC systems to achieve optimal application execution time within the power budget (Sarood et al. 2013). Power capping has been explored to reduce energy consumption in heterogeneous computing platform consisting of FPGA accelarator (Wu et al. 2016). A greedy approach is developed to maximize application performance under a power-cap limit. In (Krzywaniak and Czarnul 2019), Krzywaniak et al. explored power capping method for GPU architecture, and developed power and performance optimization method considering NVIDIA GPUs. Power and performance model for CPU and GPU based on power capping has also been explored in the literature (Komoda et al. 2013). Liu et al. proposed FastCap (Liu et al. 2016), a system-wide power capping approach based on both CPU and memory DVFS to achieve optimal system performance within a given budget for systems with a large number of cores. In this paper, we present a simulator that can predict and optimize processor power-capping values considering heterogeneous computing architecture nodes, including CPUs, GPUs, and FPGAs.

2.3 Job Scheduling Simulation

There exist many job scheduling simulators particularly focusing on HPC systems. For example, PYSS is a trace-driven HPC workload scheduling simulator written in Python (Parallel Systems Lab 2017). The simulator implements several scheduling algorithms, including a number of backfilling algorithms. Another python-based job scheduling simulator has previously been developed (Ahmed and Liu 2019). The simulator is based on Simian (Santhi et al. 2015; Chennupati et al. 2017), a parallel discrete-event simulation engine, and is focused on HPC demand response simulation based on processor frequency scaling. CQSim is another event-based simulator to study the detailed queuing behavior of job schedulers using real system

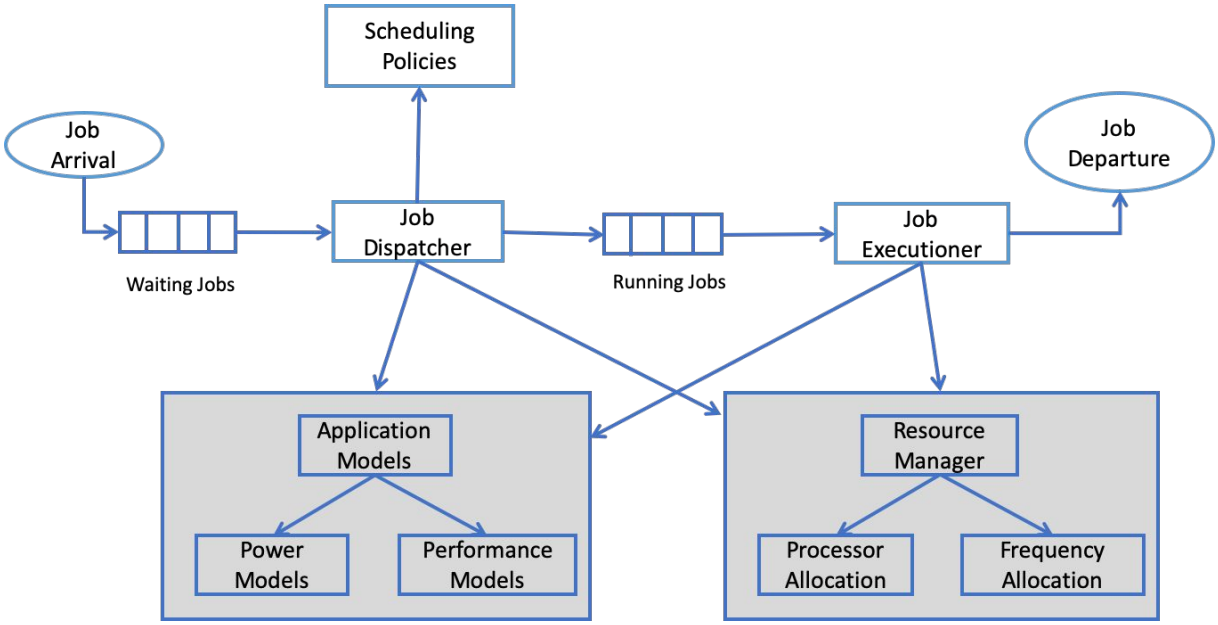


Figure 1: The simulator components.

workload (Yang et al. 2013). The structural simulation toolkit (SST) contains support for job scheduling and placement on HPC systems (Rodrigues et al. 2011; Rodrigues et al. 2012). The simulator can run multiple jobs via trace replay. CODES (Cope et al. 2011) contain a trace replay and parallel workload modeling tool to study multi-job workload of proxy applications (Acun et al. 2015). In this paper, we develop a job scheduling simulator that includes power and performance prediction and optimization model for various power-capping values.

3 SIMULATION MODEL

We develop a job scheduling simulator based on Simulus (Liu 2020), a parallel discrete-event simulation engine. Simulus supports both event-driven and process-oriented simulation world-views. It is implemented in Python with several advanced features to ease modeling and simulation tasks with both events and processes. Simulus also provides support for simultaneously running a time-synchronized group of simulators, either sequentially or in parallel. Simulus is open source and is available online. Simulus has previously been used to develop energy-efficient auction mechanism model for HPC system (Ahmed et al. 2020).

The overall simulator diagram is shown in Figure 1. The simulator will consist of five major components: a job dispatcher, a job executioner, scheduling policies, application models, and a resource manager. The job dispatcher handles different types of events, such as job arrival and job departure. After a job is submitted, it enters the job waiting queue and job dispatcher is be invoked. The job dispatcher determines which jobs to run from the waiting queue based on the scheduling policies, application models (that describes the power and performance characteristics of the jobs), and available resources from the resource manager. We present an application prediction model and resource allocation model in Section 3.1 and 3.2, respectively. When a job is scheduled to run the job dispatcher remove the job from the waiting queue and puts it in the list of running jobs. The job executioner allocates the resources using the resource manager to represent the occupied processors with associated power consumption for running the job. The job executioner then simulates the job execution. When a job completes its execution, the job executioner removes the job from the list of running jobs and reclaim the resources occupied by the job.

3.1 Power Prediction

In this subsection, we present a parallel application power prediction model. We assume that an HPC user submits job j requesting n_j nodes. Although jobs that do not use all the resources in a node exist in HPC environment, we consider only the jobs that use all the allocated nodes. The prediction model determines the power-capping value of the processors, P_j, that the job is run. Let P_{min} and P_{max} denote the minimum and maximum power-capping values for the processor running the application. That is,

$$P_{min} \leq P_j \leq P_{max}$$

We determine average power consumption p_j using the following third-order polynomial function:

$$p_j = a + b \cdot P_j + c \cdot P_j^2 + d \cdot P_j^3$$

where a, b, c, and d are constants determined from empirical analysis of average power relation with different power-capping values. In particular, a represents the static power consumption while running the application.

3.2 Resource Allocation

In this subsection, we present a resource allocation model that determines optimal resources for parallel applications. When there is a new incoming job in the system, the job scheduler in our model first checks if the job is eligible to run based on the available resources. The job is eligible to run, (a) if there are enough available processors, and (b) if the average power consumption of all running jobs remains within the power limit allocated to the HPC system, that is the following constraints are satisfied:

$$\sum_{j \in R} n_j \leq \hat{n} \tag{1}$$

$$p_j + \sum_{i \in R} p_i \leq \hat{p} \tag{2}$$

where $\hat{n}$ is the total number of processors in the system, R denotes the list that contains all the jobs that are currently running in the system, and $\hat{p}$ is the current power limit set on the HPC system (i.e., the overall power consumption by all the jobs running on the system cannot go beyond this limit). If the job is eligible to run satisfying the constraints in Equations 1 and 2, we start executing the job through allocating the required processors to run the job.

We assume the time taken for the job to execute is represented by t_j. The total energy consumption of job j can be determined as follows:

$$e_j = n_j \cdot p_j \cdot t_j$$

We determine the power-cap values for the processes based on the following optimization objective:

$$\text{Minimize} \sum_{j=1}^{n_j} e_j$$

Subject to constraints (1) and (2)

In general, the energy and power-capping observe the convexity property (Tang et al. 2016), such as a job's average power consumption and execution time are monotonic functions of the power-capping within a given range. We can therefore solve the optimization problem with the sequential least squares programming algorithm using the Han-Powell quasi-Newton method (Powell 1978) and determine the optimal power-cap values for the jobs.

4 CASE STUDIES

In this section, we present various case studies to show applicability of the prediction model and job scheduling simulator. We consider heterogeneous computing architecture for our experiments. We first present simulation results based on real-life measurements on CPU platform. We collect traces of GPU and FPGA execution of various applications from the literature. Based on the measurements, we next perform simulation studies to show effectiveness of the proposed model and simulation.

We consider the following case studies:

- **Case Study #1:** In this case study, we consider HPC applications running on CPU node. We vary the power-capping values, and measure power and performance of HPC applications running on a CPU.
- **Case Study #2:** In this case study, we consider HPC applications running on GPU node. We collect the application characteristics data from the literature (Krzywaniak and Czarnul 2019).
- **Case Study #3:** In this case study, we consider effect of power and performance on HPC applications while running on an FPGA node. We collect the application characteristics data on FPGA node from the literature (Wu et al. 2016).
- **Case Study #4:** In this case study, we consider optimal allocation of power capping values to different platform. We collect the energy consumption and runtime of the applications for optimal power-cap values.

4.1 Case Study #1

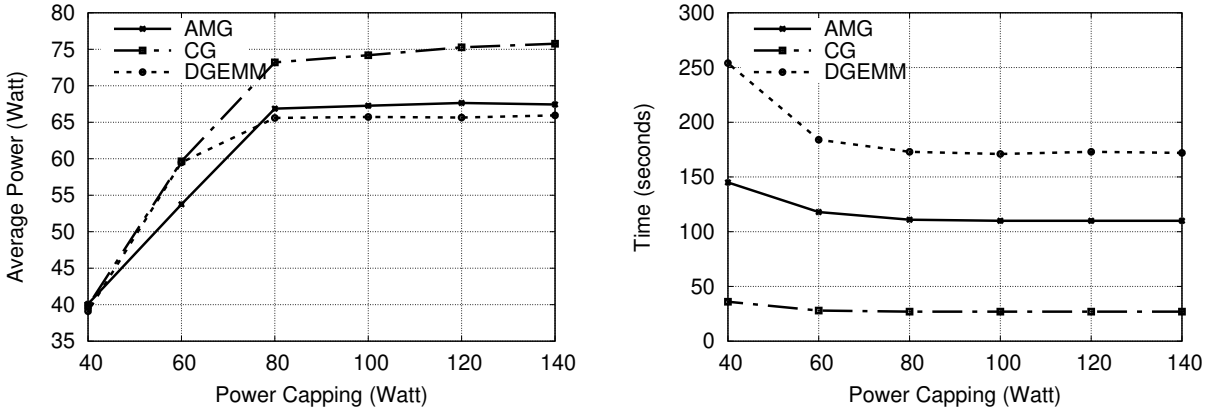
In this case study, we perform real-life measurements of HPC application power and performance for various power-capping values on CPU node. We used a system monitoring/controlling tool, called pycoolr (Ahmed et al. 2018), to measure application power, performance, and temperature. Pycoolr measures the application performance parameters using RAPL interface and reports the measurements using a javascript object notation (json) format. The tool allows upper setting of power usage on processors. Using this feature we power capped the processors, and measured performance, temperature change, and power consumption values. We varied power-cap limit from 40W to 160W, at 20W granularity, and measured various results for different applications.

We ran experiments on an Intel Sandy Bridge node with two Xeon E5-2670 processors, 8 cores, and 16 hardware threads with hyper-threading, which were run at 2.6 GHz, up to 3.3 GHz with the Intel Turbo Boost Technology. The two processors are connected via two Intel Quick Path Interconnect links, which form a cache-coherent NUMA node.

We select three applications for our experiments: AMG, DGEMM and CG application from the NAS parallel benchmark (NPB). Figure 2(a) presents the power consumption characteristics of the applications for various power-capping values. The runtime characteristics of these applications based on various power-capping values are shown in Figure 2(b).

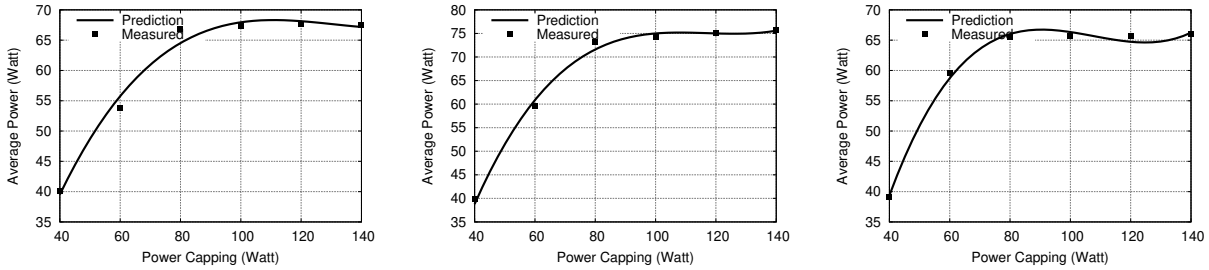
• AMG is a parallel algebraic multigrid solver for unstructured mesh grids. Figures 2(a) and 2(b) present the power consumption and execution time, respectively. The purpose of the application is to test single CPU performance and parallel scaling efficiency. AMG is written in ISO-C.It is an SPMD code which uses MPI and OpenMP threading within MPI tasks. Parallelism is achieved by data decomposition. As can be seen in the Figure 2(a), with increased power-capping limit, the power consumption increases. However, increased power-capping limit provides opportunity to execute the application faster, as can be seen in Figure 2(b).

• DGEMM is an application that measures performance for matrix-matrix multiplication. The code for the application is designed to measure the sustained, floating-point computational rate of a single node. The power and execution time measurements for DGEMM application are shown in Figures 2(a) and 2(b), respectively. As can be seen in the figures, increased power-capping limit increases power consumption of the application, while reduces the execution time of the application.



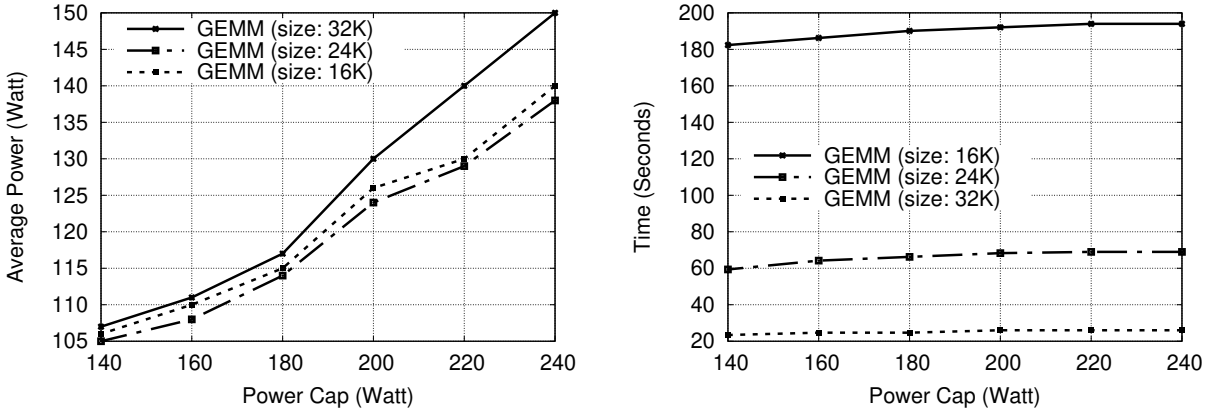
(a) Average Power (b) Execution Time

Figure 2: Measured data of three parallel applications on CPU node.



(a) AMG (b) CG (c) DGEMM

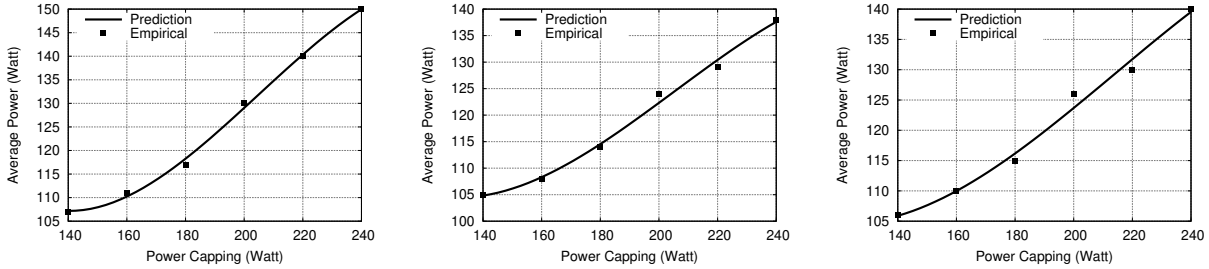
Figure 3: Power prediction model for applications running on CPU node.



(a) Average Power (b) Execution Time

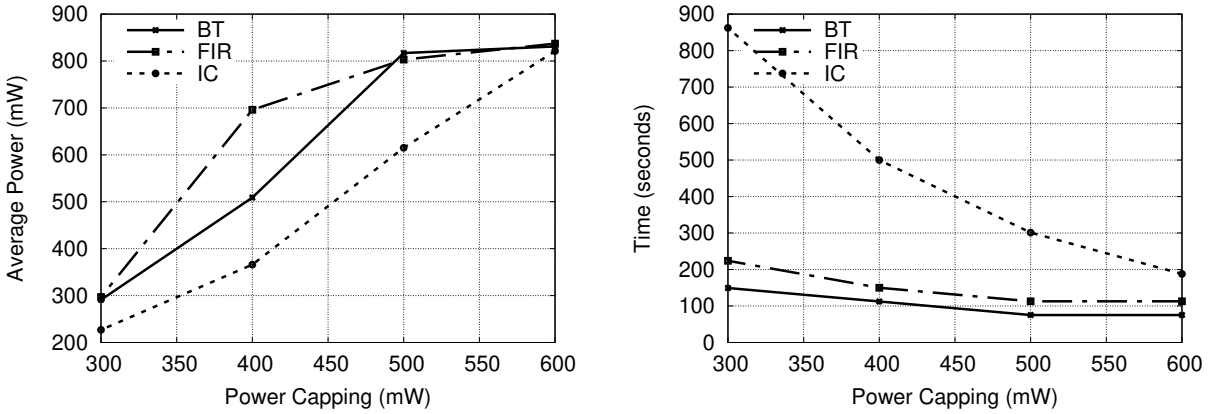
Figure 4: Empirical data of GEMM application of three different sizes on GPU node.

• The NPB suite includes a small set of programs designed to help evaluate the performance of parallel supercomputers. The benchmarks are derived from computational fluid dynamic (CFD) applications. From this suite, we selected the conjugate gradient (CG) application (class C), which uses a conjugate gradient



(a) GEMM (32K) (b) GEMM (24K) (c) GEMM (16K)

Figure 5: Power prediction model for applications running on GPU node.



(a) Average Power (b) Execution Time

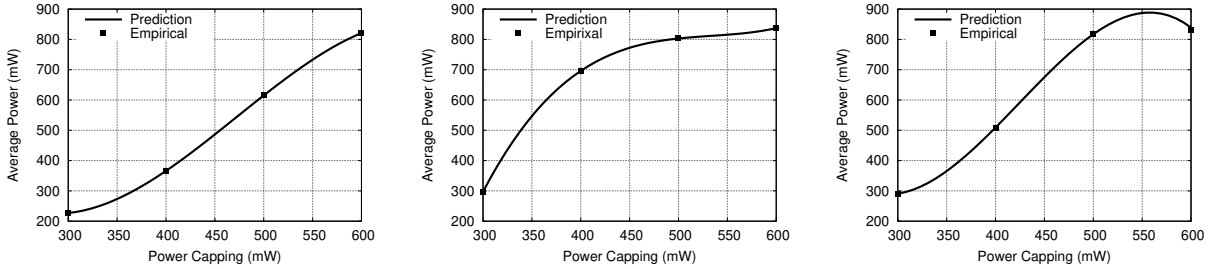
Figure 6: Empirical data of three applications on FPGA node.

algorithm for solving particular systems of linear equations. CG application execution characteristics for different power capping limits are reported in Figs. 2(a) and 2(b), respectively.

Figure 3 presents the prediction model output of different applications running on CPU node. Figures 3(a), 3(b), and 3(c) present the power consumption of applications AMG, CG, and DGEMM, respectively. Both the measured values and prediction are shown in the figures. In general, the prediction model can closely predict the power consumption of different applications for unknown power-capping values.

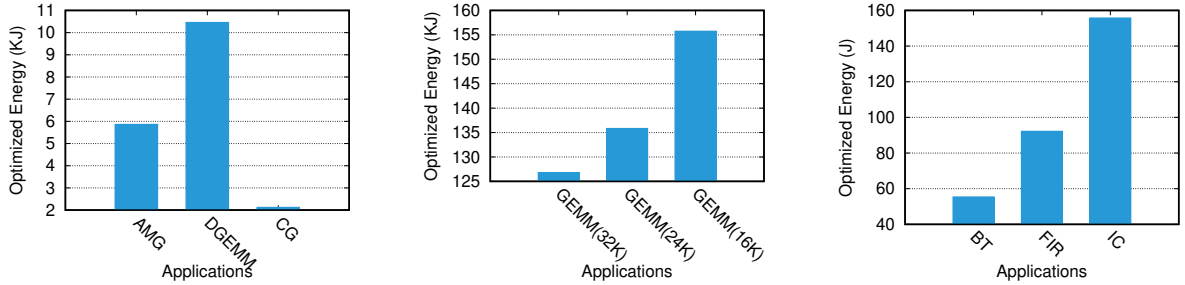
4.2 Case Study #2

In this case study, we simulate power-capping behavior of HPC applications on GPU platform. We collect and use jobs' power-related information on an NVIDIA GeForce RTX 2080 GPU platform from the literature (Krzywaniak and Czarnul 2019). We collect the power and performance data for various parallel application at different power capping values. The application used was general matrix multiplication (GEMM). The data for GEMM application for various matrix sizes (16K, 24K, and 32K) are shown in Figure 4. For this reported data, the power-capping values were changed from 140W to 240W at 20W granularity. Figure 4(a) shows the average power for different power-cap values. Increase in power-cap limit increases the power consumption for all sizes of the application. Figure 4(b) presents the application time execution for various power cap values. Increase in power-cap limit increases execution time of the application for the GPU node. The behavior is different compared to the CPU node, where application



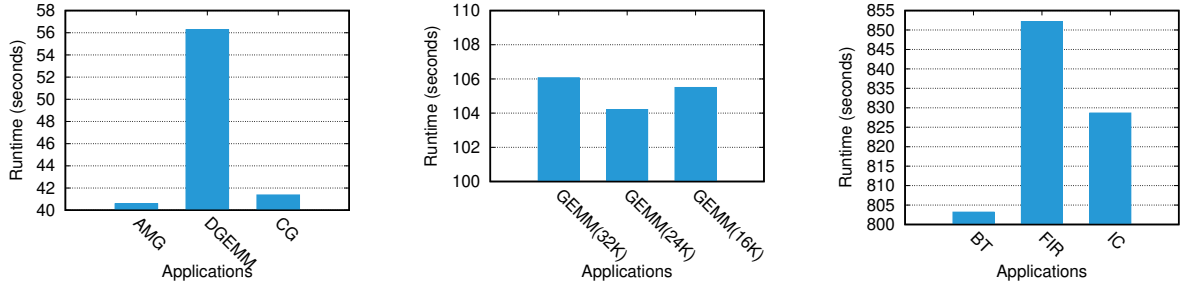
(a) BT (b) FIR (c) IC

Figure 7: Power prediction model for applications running on FPGA node.



(a) CPU (b) GPU (c) FPGA

Figure 8: Optimized energy consumption on different platforms.



(a) CPU (b) GPU (c) FPGA

Figure 9: Runtime on different platforms for optimal power-capping values.

performance improved with power-cap limit increase. Therefore, change of power-cap limit may impact differently for different computing architectures.

Figure 5 presents the prediction model output of different applications running on GPU node. We determine the parameters for each application following the prediction model as outlined in Section 3.1. Figures 5(a), 5(b), and 5(b) present the power consumption of applications GEMM (32K), GEMM (24K), and GEMM (16K), respectively. Figure 5 present both empirical data and predicted value. The prediction model of the proposed simulator can be used to predict application characteristics on GPU node for unknown power-capping values.

4.3 Case Study #3

In this case study, we simulate power-capping behavior of HPC applications on FPGA platform. We collect HPC applications' power and performance data on XC7Z020 CLG484-1 AP SoC on Zynq 702 evaluation board from (Wu et al. 2016). The HPC applications are: binomial tree vector computation (BT), finite impulse response (FIR) filter, and image convolution (IC). The data for the three application execution are shown in Figure 6. For this reported data, the reported power-capping values were changed from 300mW to 600mW at 100mW granularity. We assign 100 seconds, 150 seconds, and 250 seconds as default runtime without dynamic power-capping for the applications BT, FIR, and IC, respectively. Figure 6(a) shows the average power for different power cap values. With increase in power-capping limit, the average power consumption of different applications increase. Figure 6(b) presents the application time execution for various power-cap values. Increase in power-capping limit reduces the runtime for each application, since more power allocation allows the FPGA node to run faster.

Figure 7 presents the prediction model output of different applications running on FPGA node. Figures 7(a), 7(b), and 7(c) present the power consumption of applications BT, FIR, and IC, respectively. The prediction model of the simulator can be used to predict the application characteristics on FPGA node for various power-capping values.

4.4 Case Study #4

For this case study, we determine optimal power cap values for each application as described in Section 3.2. Figure 8 presents optimized energy consumption of different applications. Figure 8(a) presents the optimized energy consumption using the CPU platform for three applications: AMG, DGEMM, and CG from NPB benchmark. Figs. 8(b) and 8(c) present optimized energy consumption for GPU and FPGA platforms, respectively. The optimal power-capping value for this experiment is determined using the resource allocation module of the simulator as described in Section 3.2. Figure 9 presents the application runtime for optimal power-cap values. Figures 9(a), 9(b), and 9(c) present the runtime of different applications on CPU, GPU and FPGA, respectively. Our resource allocation model can be used to determine the optimal power-capping values to run parallel applications on heterogeneous computing platform.

5 CONCLUSION

In this paper, we present a simulator for parallel application simulation and performance prediction. Our simulator is developed based on a discrete event simulation engine. The simulator includes a power and performance prediction model, as well as a resource allocation model. The prediction model can predict power and performance for various power-capping values. The resource allocation model allocates power-capping values optimally to parallel applications. We present different case studies to show the application of the developed simulator. We consider heterogeneous computing architecture (CPUs, GPUs and FPGAs) for simulation. We present real-life measurements of application power and performance for various power-capping values on CPU node. We collect trace data of power and performance on GPU and FPGA node. Based on real-life measurements and trace-based data we show prediction and optimization capability of our proposed simulator.

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